

REMARKS/ARGUMENTS

Claims 1-21 are pending in the application. Claims 1, 3, 9, 12, and 18-20 are amended herein. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

On page 2 of the office action, the Examiner asked the Applicant to check the 1449 form completed by the Examiner for accuracy. In response, the Applicant submits the completed 1449 form appears to be accurate.

On page 2, the Examiner objected to claims 3-7 and 12-18 because of informalities. In response, the Applicant has amended claims 3 and 12 to recite "programmable accuracy level," instead of "user-programmable accuracy level" to conform with the recitations in claims 1 and 9.

On page 2, the Examiner rejected claims 9 and 19 under 35 U.S.C. 102(b) as being anticipated by Foley. On page 3, the Examiner rejected claims 1-2, 9-11, and 19 under 35 U.S.C. 103(a) as being unpatentable over Kaenel in view of Foley and Greenfield. On page 5, the Examiner objected to claims 3-8, 12-18, and 20 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. On page 5, the Examiner stated that claim 21 is allowable over the art of record. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over the cited references.

Claims 1, 9, and 19

Claim 1 has been amended to clarify that the PLDC circuit receives an input control signal specifying one of a plurality of different possible input control values, each input control value corresponding to one of a plurality of different possible programmable accuracy levels. Claim 1 has been further amended to clarify that the PLDC circuit is adapted to determine whether operations of the clock generator have settled to a stable operating point to within the programmable accuracy level corresponding to the input control value specified by the input control signal.

In rejecting claim 1, the Examiner proposed two separate arguments as to why the cited references teach the "programmable accuracy level" recited in original claim 1.

The first argument was based on an interpretation of the term "programmable" such that the accuracy level employed by the device of Foley was said to be a "programmable" accuracy level, because "the device of Foley has been preprogrammed via the selection of the various logic elements."

To address this argument, the Applicant has amended claim 1 to distinguish the claimed invention from the teachings in Foley. According to currently amended claim 1, the PLDC receives an input control signal specifying one of a plurality of different possible input control values, each input control value corresponding to one of a plurality of different possible programmable accuracy levels, where the PLDC circuit is adapted to determine whether operations of the clock generator have settled to a stable operating point to within the programmable accuracy level corresponding to the input control value specified by the input control signal. Foley does not teach or even suggest such a combination of features.

The second argument was based on the assertion that "hard-wired devices can be implemented via a microprocessor thereby allowing the program of the hard-wired devices to be changed," citing Greenfield. Based on that assertion, the Examiner concluded that "it would have been obvious ... to have

formed any of the hard-wired devices [taught in Foley and Kaenel] via a microprocessor because of the art recognized equivalence of these structures." For the following reasons, the Applicant submits that the Examiner's second argument is improper.

On page 10, Greenfield teaches: "Any function that can be implemented using hard-wired digital ICs can also be implemented or performed by a μ C." Applying this teaching to the teachings in Foley and Kaenel would yield microprocessor-based devices that implement the exact same functions implemented by the hard-wired devices of Foley and Kaenel. Such a combination of teachings would not provide a microprocessor-based device that implements all of the functions of the hard-wired devices of Foley and Kaenel plus the additional function of receiving an input control signal specifying one of a plurality of different possible input control values, each input control value corresponding to one of a plurality of different possible programmable accuracy levels.

Moreover, just because functions can be implemented in software on a microprocessor rather than in hardware on a digital IC, that does not mean that that software necessarily makes every fixed value corresponding to the hardware implementation a programmable value in the software implementation. In order for such a conclusion to be a proper grounds for rejecting a claim in a U.S. patent application, there has to be a suggestion in the prior for changing that fixed value into a programmable value.

As stated above, the Examiner cited Greenfield in support of his assertion that "hard-wired devices can be implemented via a microprocessor thereby allowing the program of the hard-wired devices to be changed." Significantly, however, while Greenfield clearly teaches that "hard-wired devices can be implemented via a microprocessor," Greenfield does not say anything about changing the functions of those hard-wired devices. And neither do any of the other cited references of record.

Furthermore, without a suggestion in the prior art for changing the fixed accuracy level of Foley into a programmable value, there would be no motivation to implement the hard-wired device of Foley as a microprocessor-based device. After all, as Greenfield explicitly teaches, starting at the bottom of page 10, there are still many significant advantages that hard-wired logic maintains over microprocessors.

The Applicant emphasizes that the issue is not whether the prior art teaches "hard-wired" devices or "microprocessor-based" devices. The issue is whether the prior art teaches devices that support the recited "programmable accuracy level." Significantly, embodiments of the present invention are described in the specification in the context of field-programmable gate arrays (FPGAs), which are different from both the hard-wired devices and the microprocessor-based devices discussed in Greenfield.

In view of the foregoing, the Applicant submits that the Examiner's second argument for rejecting claim 1 is improper and is, in any case, overcome by the amendments made to claim 1.

For all these reasons, the Applicant submits that currently amended claim 1 is allowable over the cited references. For similar reasons, the Applicant submits that currently amended claims 9 and 19 are allowable over the cited references. Since claims 2-8, 10-18, and 20 depend variously from claims 1, 9, and 19, it is further submitted that those claims are also allowable over the cited references. The Applicant submits therefore that the rejections of claims under Sections 102(b) and 103(a) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

Date: 3/15/05
Customer No. 22186
Mendelsohn & Associates, P.C.
1515 Market Street, Suite 715
Philadelphia, Pennsylvania 19102

Steve Mendelsohn
Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)